



LDC1000 电感数字转换器

1 特性

- 无磁体操作
- 亚微米高精度
- 可调节感测范围（通过线圈设计实现）
- 系统成本较低
- 支持远程放置传感器（在恶劣环境中对 LDC 去耦合）
- 高耐用性（通过非接触式操作实现）
- 不易受到环境干扰因素的影响（诸如污垢、灰尘、水、油）
- 电源电压范围（模拟）：4.75V 至 5.25V
- 电源电压范围 (I/O)：1.8V 至 5.25V
- 电源电流（不含 LC 振荡电路）：1.7mA
- R_p 分辨率：16 位
- L 分辨率：24 位
- LC 频率范围：5kHz 至 5MHz

2 应用

- 位置感测
- 运动感测
- 轮齿计数
- 流量计
- 按钮开关
- 多功能打印机
- 数码照相机
- 医疗设备

3 说明

电感感测是一种遥控的、短程感测技术，此项技术能够在灰尘、污垢、油和潮湿环境中实现导体目标的低成本、高分辨率感测，这使得它在恶劣环境中非常可靠。通过使用可在印刷电路板 (PCB) 上被创建为一个感测元件的线圈，LDC1000 可实现超低成本系统解决方案。

电感感测技术可对线性位置或角位置、位移、运动、压缩、振动、金属成分及其他应用进行高精度测量，广泛应用于汽车、消费类产品、计算机、工业、医疗和通信等市场领域。与同类感测技术相比，电感感测的性能更为优异，可靠性和灵活性更高并且系统成本更低。

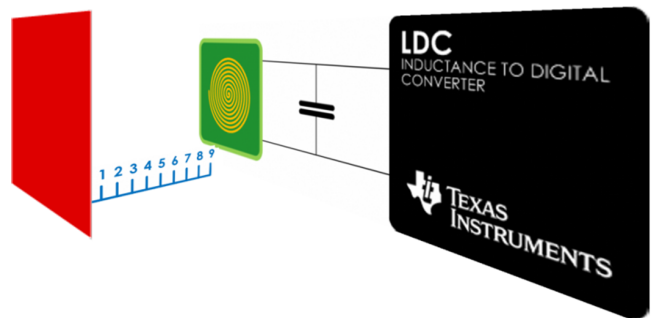
LDC1000 是世界上第一个电感数字转换器，从而在一个低功耗、小封装尺寸解决方案内提供电感感测的优势。此产品采用一个小外形尺寸无引线 (SON)-16 封装，并且提供了几种运行模式。其串行外设接口 (SPI) 简化了与微控制器 (MCU) 的连接方式。

器件信息⁽¹⁾

| 部件号 | 封装 | 封装尺寸（标称值） |
|---------|-----------|-----------------|
| LDC1000 | WSON (16) | 5.00mm × 4.00mm |

(1) 如需了解所有可用封装，请参见数据表末尾的可订购产品附录。

轴距感测应用



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4 修订历史记录

| Changes from Revision B (March 2015) to Revision C | Page |
|---|------|
| • Changed XOUT pin description to clarify proper crystal connection | 4 |
| • Added instructions on proper DAP connection | 4 |
| • Added conditions for L measurement resolution | 6 |
| • Changed TYP to NOM | 7 |
| • Changed Some descriptions of device functionality for better clarity and consistency | 9 |
| • Changed RP Conversion equation for clarity | 12 |
| • Added extended SPI transaction figure for clarity | 17 |
| • Changed Register maps to include Clock Configuration and Threshold Registers | 18 |
| • Changed description of Min Sensor frequency for clarity | 21 |
| • Added documentation of registers 0x05, 0x06, and 0x08 | 21 |
| • Changed description of OSC Status to include possible causes | 23 |
| • Changed some details on Application Information for improved clarity and consistency | 24 |
| • Deleted lateral and rotation images from example applications, as example application details axial sensing configuration | 25 |
| • Changed details of example design for improved clarity | 26 |

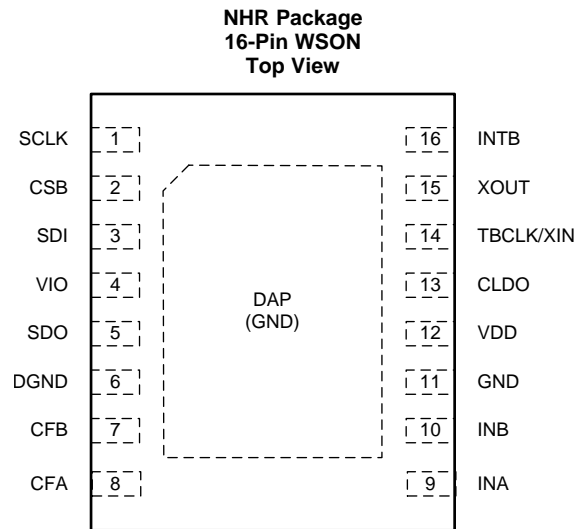
| Changes from Revision A (December 2013) to Revision B | Page |
|---|------|
| • 已添加 ESD 额定值表, 特性描述部分, 器件功能模式, 应用和实施部分, 电源相关建议部分, 布局部分, 器件和文档支持部分以及机械、封装和可订购信息部分 | 1 |
| • Changed SCLK Pin type from DO to DI | 4 |
| • Added L Res value to <i>Electrical Characteristics</i> | 6 |
| • Added <i>Measuring Inductance With LDC1000</i> subsection to <i>Feature Description</i> | 12 |
| • Changed Frequency Counter Data values in Register Description table | 18 |

Changes from Original (September 2013) to Revision A

Page

| | |
|-----------------------------|-------------------|
| • Changed SCLK to CSB | 7 |
|-----------------------------|-------------------|

5 Pin Configuration and Functions



Pin Functions

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|-----------|-----|---------------------|--|
| NAME | NO. | | |
| SCLK | 1 | DI | SPI clock input. SCLK is used to clock-out/clock-in the data from/into the chip |
| CSB | 2 | DI | SPI CSB. Multiple devices can be connected on the same SPI bus with each device having a dedicated CSB connection to the MCU so that each device can be uniquely selected. |
| SDI | 3 | DI | SPI Slave Data In (Master Out Slave In). This should be connected to the Master Out Slave In of the master |
| VIO | 4 | P | Digital IO Supply |
| DGND | 6 | P | Digital ground |
| SDO | 5 | DO | SPI Slave Data Out (Master In Slave Out). It is Hi-Z when CSB is high |
| CFB | 7 | A | LDC filter capacitor |
| CFA | 8 | A | LDC filter capacitor |
| INA | 9 | A | External LC Tank. Connected to external LC tank |
| INB | 10 | A | External LC Tank. Connected to external LC tank |
| GND | 11 | P | Analog ground |
| VDD | 12 | P | Analog supply |
| CLDO | 13 | A | LDO bypass capacitor. A 56 nF capacitor should be connected from this pin to GND |
| TBCLK/XIN | 14 | DI/A | External time-base clock/XTAL. Either an external clock or crystal can be connected. |
| XOUT | 15 | A | XTAL. Crystal out. When using a crystal, a crystal should be connected across XIN and XOUT. When not using a crystal, this pin should be left floating. |
| INTB | 16 | DO | Configurable interrupt output. |
| DAP | 17 | P | Connect to GND for improved thermal performance. ⁽²⁾ |

(1) DO: Digital Output, DI: Digital Input, P: Power, A: Analog

(2) There is an internal electrical connection between the exposed Die Attach Pad (DAP) and the GND pin of the device. Although the DAP can be left floating, for best performance the DAP should be connected to the same potential as the device's GND pin. Do not use the DAP as the primary ground for the device. The device GND pin must always be connected to ground.

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

| | MIN | MAX | UNIT |
|--|------|----------------|------|
| Analog Supply Voltage ($V_{DD} - GND$) | | 6 | V |
| IO Supply Voltage ($V_{IO} - GND$) | | 6 | V |
| Voltage on any Analog Pin | −0.3 | $V_{DD} + 0.3$ | V |
| Voltage on any Digital Pin | −0.3 | $V_{IO} + 0.3$ | V |
| Input Current on INA and INB | | 8 | mA |
| Junction Temperature, T_J ⁽²⁾ | | 150 | °C |
| Storage temperature, T_{stg} | −65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A . The maximum allowable power dissipation at any ambient temperature is $P_{DMAX} = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board. The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 ESD Ratings

| | | VALUE | UNIT |
|-------------------------------------|--|-------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±1000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±250 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Condition⁽¹⁾

| | MIN | NOM | MAX | UNIT |
|--|------|-----|------|------|
| Analog Supply Voltage ($V_{DD} - GND$) | 4.75 | | 5.25 | V |
| IO Supply Voltage ($V_{IO} - GND$) | 1.8 | | 5.25 | V |
| $V_{DD} - V_{IO}$ | ≥0 | | | V |
| Operating Temperature, T_A | −40 | | 125 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | LDC1000 | UNIT |
|-------------------------------|---|------------|------|
| | | NHR (WSON) | |
| | | 16-PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance ⁽²⁾ | 28 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

- (2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A . The maximum allowable power dissipation at any ambient temperature is $P_{DMAX} = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board. The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_A = T_J = 25^\circ\text{C}$, $V_{DD} = 5.0\text{ V}$, $V_{IO} = 3.3\text{ V}^{(1)(2)}$

| PARAMETER | | TEST CONDITIONS | MIN ⁽³⁾ | TYP ⁽⁴⁾ | MAX ⁽³⁾ | UNIT |
|---|--|---|---------------------|---------------------|--------------------|----------------|
| POWER | | | | | | |
| V_{DD} | Analog Supply Voltage | | 4.75 | 5 | 5.25 | V |
| V_{IO} | IO Supply Voltage | $V_{IO} \leq V_{DD}$ | 1.8 | 3.3 | 5.25 | V |
| I_{DD} | Supply Current on VDD pin | PWR_MODE = 1, no sensor connected | | 1.7 | 2.3 | mA |
| I_{VIO} | IO Supply Current | Static current | | | 14 | μA |
| I_{DD_LP} | Standby Mode Supply Current on VDD pin | PWR_MODE = 0, no sensor connected | | 250 | | μA |
| t_{START} | Start-Up Time | From POR to ready-to-convert. Crystal not used for frequency counter | | 2 | | ms |
| LDC | | | | | | |
| f_{SENSOR_MIN} | Minimum sensor frequency | | | 5 | | kHz |
| f_{SENSOR_MAX} | Maximum sensor frequency | | | 5 | | MHz |
| A_{SENSOR_MIN} | Minimum sensor amplitude | | | 1 | | V_{PP} |
| A_{SENSOR_MAX} | Maximum sensor amplitude | | | 4 | | V_{PP} |
| t_{REC} | Recovery time | Oscillation start-up time after R_P under-range condition | | 10 | | $1/f_{sensor}$ |
| R_{P_MIN} | Minimum Sensor R_P Range | | | 798 | | Ω |
| R_{P_MAX} | Maximum Sensor R_P Range | | | 3.93 | | M Ω |
| R_{P_RES} | R_P Measurement Resolution | | | 16 | | Bits |
| L Res | Inductance Measurement Resolution | RESPONSE_TIME = b111 (6144), $f_{EXT} = 8\text{ MHz}$, $f_{SENSOR} = 5\text{ kHz}$ | | 24 | | Bits |
| t_{S_MIN} | Minimum Response Time | Minimum programmable settling time of digital filter | | $192/f_{SE_NSOR}$ | | s |
| t_{S_MAX} | Maximum Response Time | Maximum programmable settling time of digital filter | | $6144/f_{S_ENSOR}$ | | s |
| EXTERNAL CLOCK/CRYSTAL FOR FREQUENCY COUNTER | | | | | | |
| Crystal | Frequency | | | 8 | | MHz |
| | Startup time | | | 30 | | ms |
| External Clock | Frequency | | | | 8 | MHz |
| | Clock Input High Voltage | | | | V_{IO} | V |
| DIGITAL I/O CHARACTERISTICS | | | | | | |
| V_{IH} | Logic 1 Input Voltage | | $0.8 \times V_{IO}$ | | | V |
| V_{IL} | Logic 0 Input Voltage | | | $0.2 \times V_{IO}$ | | V |
| V_{OH} | Logic 1 Output Voltage | $I_{SOURCE} = 400\text{ }\mu\text{A}$ | | $V_{IO} - 0.3$ | | V |
| V_{OL} | Logic 0 Output Voltage | $I_{SINK} = 400\text{ }\mu\text{A}$ | | | 0.3 | V |
| I_{IOHL} | Digital IO Leakage Current | | -500 | | 500 | nA |

- (1) [Electrical Characteristics](#) table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. [Absolute Maximum Ratings](#) indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
- (2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A . The maximum allowable power dissipation at any ambient temperature is $P_{DMAX} = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board. The package thermal impedance is calculated in accordance with JESD 51-7.
- (3) Limits are specified by testing, design, or statistical analysis at 25°C . Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
- (4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

6.6 Timing Requirements

Unless otherwise noted, all limits specified at TA = 25°C, VDD=5.0, VIO=3.3, 10 pF capacitive load in parallel with a 10 kΩ load on SDO. Specified by design; not production tested.

| | | MIN | NOM | MAX | UNIT |
|--------------------|-----------------------------|--|-------------------------|-----|------|
| f_{SCLK} | Serial Clock Frequency | | | 4 | MHz |
| t_{PH} | SCLK Pulse Width High | $f_{\text{SCLK}} = 4 \text{ MHz}$ | $0.4 / f_{\text{SCLK}}$ | | s |
| t_{PL} | SCLK Pulse Width Low | $f_{\text{SCLK}} = 4 \text{ MHz}$ | $0.4 / f_{\text{SCLK}}$ | | s |
| t_{SU} | SDI Setup Time | 10 | | | ns |
| t_{H} | SDI Hold Time | 10 | | | ns |
| t_{ODZ} | SDO Driven-to-Tristate Time | Measured at 10% / 90% point | | 20 | ns |
| t_{OZD} | SDO Tristate-to-Driven Time | Measured at 10% / 90% point | | 20 | ns |
| t_{OD} | SDO Output Delay Time | | | 20 | ns |
| t_{CSS} | CSB Setup Time | 20 | | | ns |
| t_{CSH} | CSB Hold Time | 20 | | | ns |
| t_{IAG} | Inter-Access Gap | 100 | | | ns |
| t_{DRDYB} | Data ready pulse width | Data ready pulse at every 1 / ODR if no data is read | $1 / f_{\text{sensor}}$ | | s |

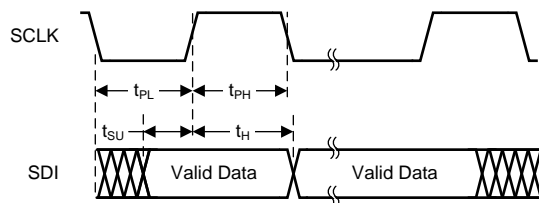


Figure 1. Write Timing Diagram

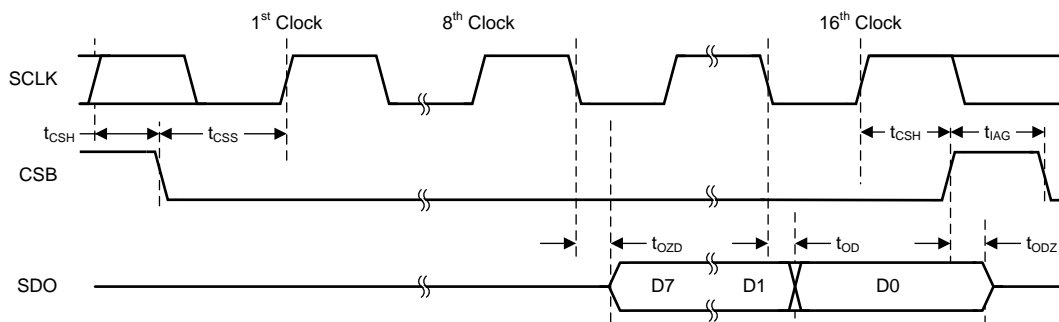
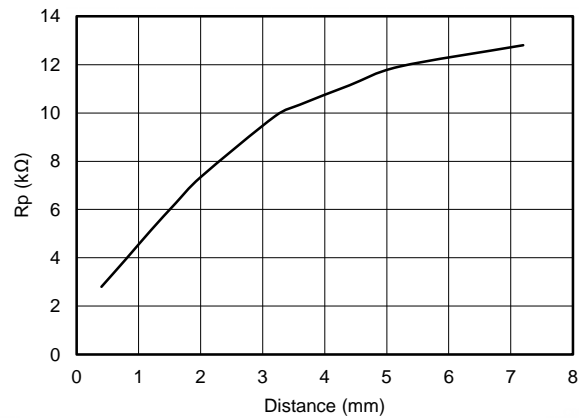


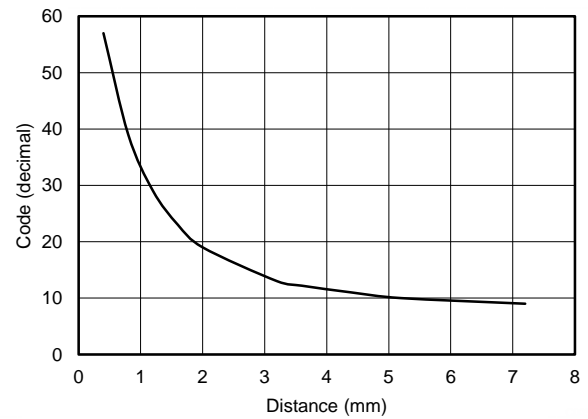
Figure 2. Read Timing Diagram

6.7 Typical Characteristics



Sensor Details: [Table 23](#)
 Target: Stainless
 Material: Steel
 R_{p_MIN} : 1.347 kΩ
 R_{p_MAX} : 38.785 kΩ

Figure 3. R_p vs Distance



Sensor Details: [Table 23](#)
 Target: Stainless
 Material: Steel
 R_{p_MIN} : 1.347 kΩ
 R_{p_MAX} : 38.785 kΩ

Figure 4. Proximity Data vs Distance

7 Detailed Description

7.1 Overview

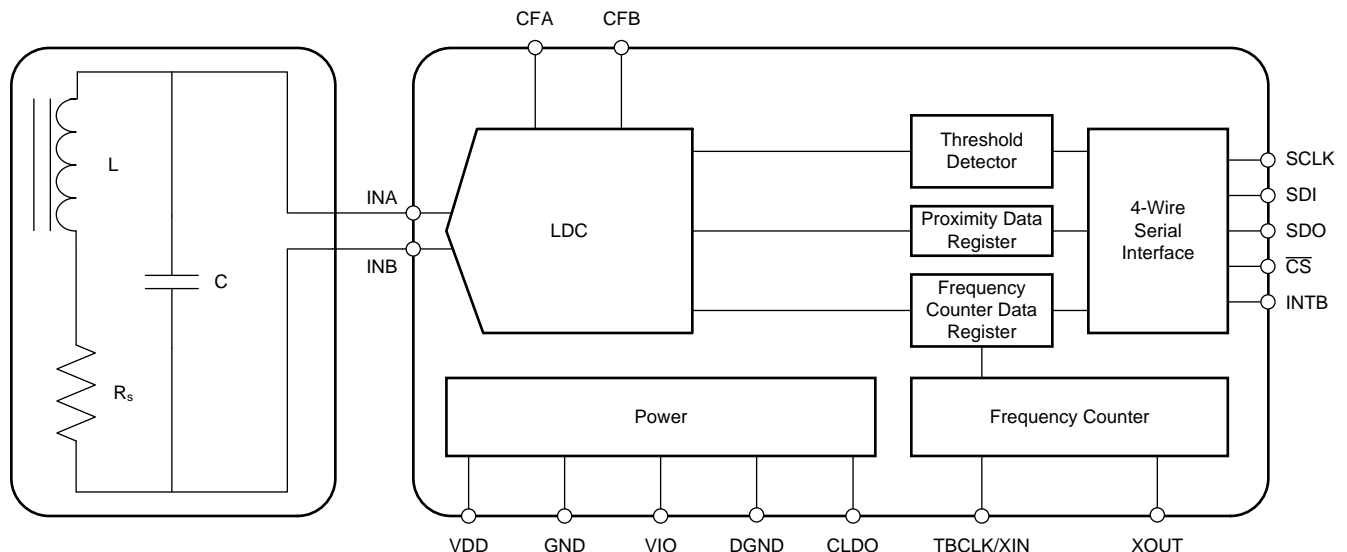
The LDC1000 is an Inductance-to-Digital Converter that measures the parallel impedance of an LC resonator. It accomplishes this task by regulating the oscillation amplitude in a closed-loop configuration to a constant level, while monitoring the energy dissipated by the resonator. By monitoring the amount of power injected into the resonator, the LDC1000 can determine the value of R_p ; it returns this as a digital value which is inversely proportional to R_p .

The threshold detector block provides a comparator with hysteresis. With the threshold registers programmed and comparator enabled, proximity data register is compared with threshold registers and INTB pin indicates the output.

The device has a simple 4-wire SPI interface. The INTB pin provides multiple functions which are programmable with SPI.

The device has separate supplies for Analog and I/O, with analog operating at 5 V and I/O at 1.8-5 V. The integrated LDO needs a 56 nF capacitor connected from CLDO pin to GND.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Inductive Sensing

An AC current flowing through an inductor will generate an AC magnetic field. If a conductive material, such as a metal target, is brought into the vicinity of the coil, this magnetic field will induce circulating currents (eddy currents) on the surface of the target. These eddy currents are a function of the distance, size, and composition of the target. The eddy currents then generate their own magnetic field, which opposes the original field generated by the coil. This mechanism is best compared to a transformer, where the coil is the primary core and the eddy current is the secondary core. The inductive coupling between both cores depends on distance and shape. Hence the resistance and inductance of the secondary core (eddy current), shows up as a distant dependent resistive and inductive component on the primary side (coil). The figures (Figure 5 to Figure 8) below show a simplified circuit model.

Feature Description (continued)

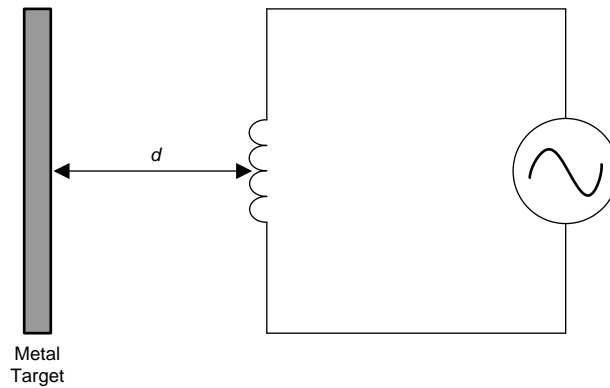


Figure 5. Inductor With a Metal Target

Eddy currents generated on the surface of the target can be modeled as a transformer as shown in [Figure 6](#). The coupling between the primary and secondary coils is a function of the distance and the conductor's characteristics. In [Figure 6](#), the inductance L_S is the coil's inductance, and R_S is the coil's parasitic series resistance. The inductance $L(d)$, which is a function of sensor to target distance, d , is the coupled inductance of the metal target. Likewise, $R(d)$ is the parasitic resistance of the eddy currents and is also a function of distance.

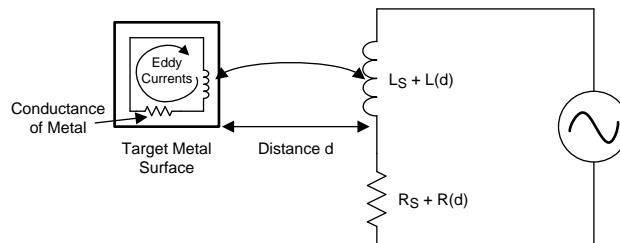


Figure 6. Metal Target Modeled as L and R With Circulating Eddy Currents

Generating an alternating magnetic field with just an inductor will consume a large amount of power. This power consumption can be reduced by adding a parallel capacitor, turning it into a resonator as shown in [Figure 7](#). In this manner the power consumption is reduced to the eddy and inductor losses $R_S + R(d)$ only.

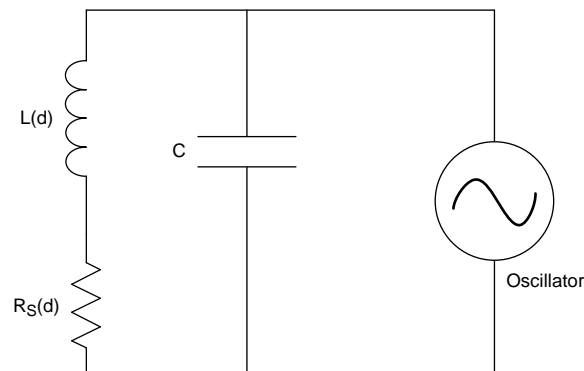


Figure 7. LC Tank Connected to Oscillator

Feature Description (continued)

The LDC1000 doesn't measure the series resistance directly; instead it measures the equivalent parallel resonance impedance R_P (see Figure 8). This representation is equivalent to the one shown in Figure 8, where the parallel resonance impedance $R_P(d)$ is given by:

$$R_P(d) = \frac{L_S + L(d)}{[R_S + R(d)] \times C} \quad (1)$$

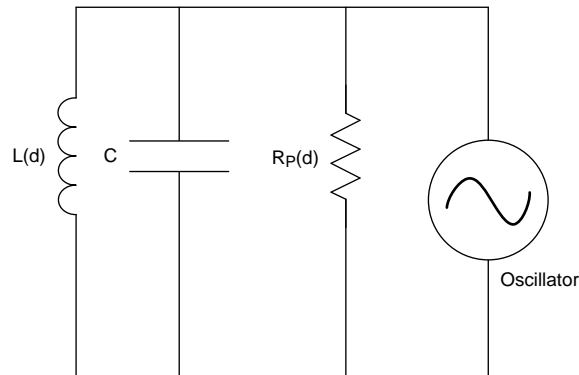


Figure 8. Equivalent Resistance of R_S in Parallel With LC Tank

Figure 9 below shows the variation in R_P as a function of distance for a 14 mm diameter PCB coil (refer to Sensor Details: Table 23). The target in this example is a section of a 2 mm thick stainless steel disk.

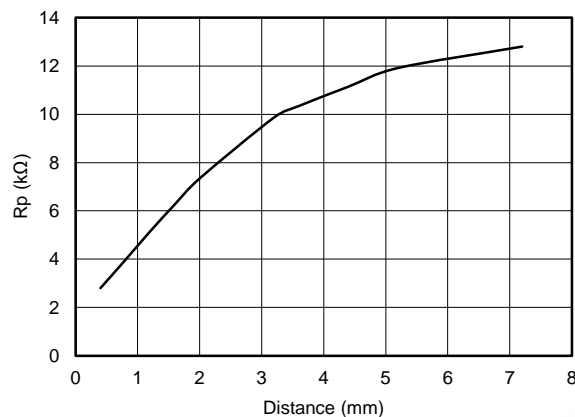


Figure 9. Typical R_P vs Distance With 14-mm PCB Coil

7.3.2 Measuring R_P With LDC1000

The LDC1000 supports a wide range of LC combinations, with oscillation frequencies ranging from 5 kHz to 5 MHz and R_P ranging from 798 Ω to 3.93 M Ω . This range of R_P can be viewed as the maximum input range of an ADC. As illustrated in Figure 9, the range of R_P is typically much smaller than the maximum input range supported by the LDC1000. To get better resolution in the desired sensing range, the LDC1000 offers a programmable input range through the R_{P_MIN} and R_{P_MAX} registers. Refer to [Calculation of \$R_{P_MIN}\$ and \$R_{P_MAX}\$](#) for information on setting these registers.

When the resonance impedance R_P of the sensor drops below the programed R_{P_MIN} , the R_P output of the LDC will clip at its full scale output. This situation could, for example, happen when a target comes too close to the coil.

Feature Description (continued)

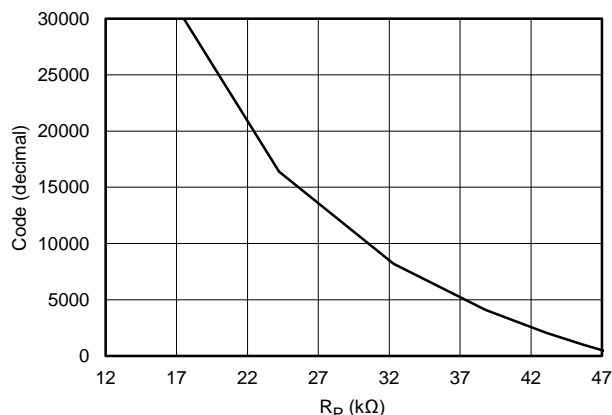


Figure 10. Transfer Characteristics of LDC1000 With R_P_MIN = 16.160 kΩ and R_P_MAX = 48.481 kΩ

The resonance impedance can be calculated from the digital output code as follows:

$$R_P = \frac{R_{P_MAX} \times R_{P_MIN}}{[R_{P_MIN} \times (1 - Y)] + (R_{P_MAX} \times Y)}$$

Where:

- R_P = Measured sensor parallel resistance in kΩ.
- R_P_MIN is the resistance (in kΩ) selected in register 0x02
- R_P_MAX is the resistance (in kΩ) selected in register 0x01
- Y = Proximity Data ÷ 2¹⁵
- Proximity data is the LDC R_P output = (Contents of Register 0x22) × 2⁸ + (Contents of register 0x21). (2)

Example: If Proximity data (address 0x22:0x21) is 5000, R_P_MIN is 2.394 kΩ, and R_P_MAX is 38.785 kΩ, the resonance impedance is given by:

$$Y = 5000/2^{15} = 0.1526$$

$$R_P = (38785 \times 2394) \div (2394 \times (1 - 0.1526) + 38785 \times 0.1526) = (92851290 \div (2028.675 + 5918.591))$$

$$R_P = 11.683 \text{ k}\Omega$$

7.3.3 Measuring Inductance With LDC1000

LDC1000 measures the sensor's frequency of oscillation using a frequency counter. The frequency counter timing is set by an external clock applied on TBCLK pin. The sensor frequency can be calculated from the frequency counter register value (see registers 0x23 through 0x25) as follows:

$$f_{\text{SENSOR}} = \frac{f_{\text{EXT}} \times \text{RESPONSE_TIME}}{3 \times \text{FCOUNT}}$$

Where:

- f_{SENSOR} is the measured sensor frequency
- f_{EXT} is the frequency of the external clock.
- FCOUNT is the value obtained from the Frequency Counter Data registers (address 0x23, 0x24, 0x25).
- RESPONSE_TIME is the programmed response time (set in the LDC configuration register, address 0x04). (3)

Feature Description (continued)

The sensor inductance can be determined by:

$$L = \frac{1}{C \times (2\pi \times f_{\text{SENSOR}})^2}$$

where

- C is the parallel sensor capacitance
- f_{SENSOR} is the sensor frequency calculated in [Equation 3](#) (4)

Example: If $f_{\text{EXT}} = 6\text{MHz}$, $\text{RESPONSE_TIME} = 6144$, $C = 100\text{ pF}$ and measured $F_{\text{count}} = 3000$ (dec) (address 0x23 through 0x25)

$$f_{\text{sensor}} = (1/3) \times (6000000/3000) \times (6144) = 4.096\text{ MHz}$$

$$\text{Now using, } L = \frac{1}{C \times (2\pi \times f_{\text{SENSOR}})^2}$$

The sensor inductance $L = 15.098\text{ }\mu\text{H}$.

The accuracy of a measurement largely depends upon the frequency of the external time-base clock (TBCLK). A higher frequency will provide better measurement accuracy. The maximum supported frequency is 8 MHz.

7.4 Device Functional Modes

7.4.1 Power Modes

The LDC1000 has two power modes:

- **Active Mode:** In this mode the LDC1000 is performing conversions. Changing any device configuration settings except PWR_MODE or INTB_MODE when the LDC1000 is in active mode is not recommended. This mode is selected when $\text{PWR_MODE} = 1$.
- **Standby Mode:** This is the default mode on device power-up. In the mode the LDC1000 power consumption is lower than when in Active mode, however the LDC1000 is not performing conversions. The device's SPI is enabled and the device should be configured in this mode. This mode is selected when $\text{PWR_MODE} = 0$.

7.4.2 INTB Pin Modes

The INTB pin is a configurable output pin which can be used to drive an interrupt on an MCU. This mode is selected by setting INTB_MODE . The LDC1000 provides three different modes on INTB pin:

1. Comparator Mode
2. Wake-Up Mode
3. DRDY Mode

LDC1000 has a built-in High and Low trigger threshold which registers as a comparator with programmable hysteresis or a special mode which can be used to wake up an MCU. These modes are explained in detail below.

7.4.2.1 Comparator Mode

In the Comparator mode, the INTB pin is asserted or deasserted when the proximity register value increases above Threshold High or decreases below Threshold Low registers respectively. In this mode, the LDC1000 essentially behaves as a proximity switch with programmable hysteresis.

Device Functional Modes (continued)

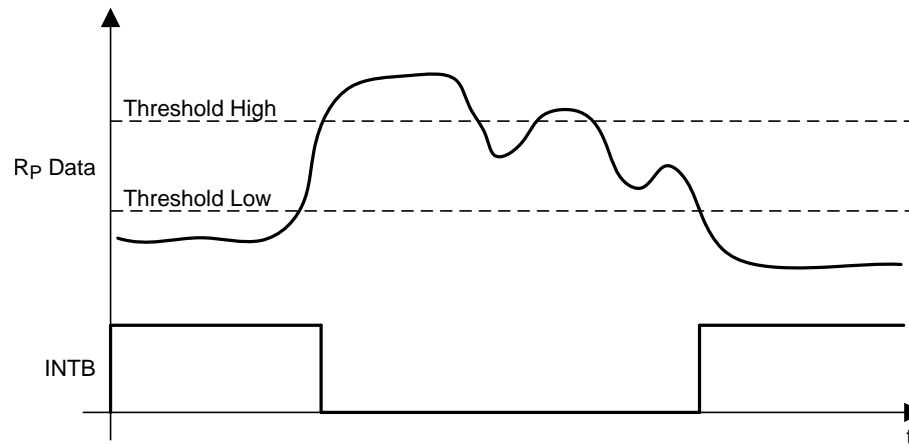


Figure 11. Behavior of INTB Pin in Comparator Mode

Device Functional Modes (continued)

7.4.2.2 Wake-Up Mode

In Wake-up mode, the INTB pin is asserted when proximity register value increases above Threshold High and deasserted when wake-up mode is disabled in INTB pin mode register.

This mode can be used to wake up an MCU which is asleep, to conserve power.

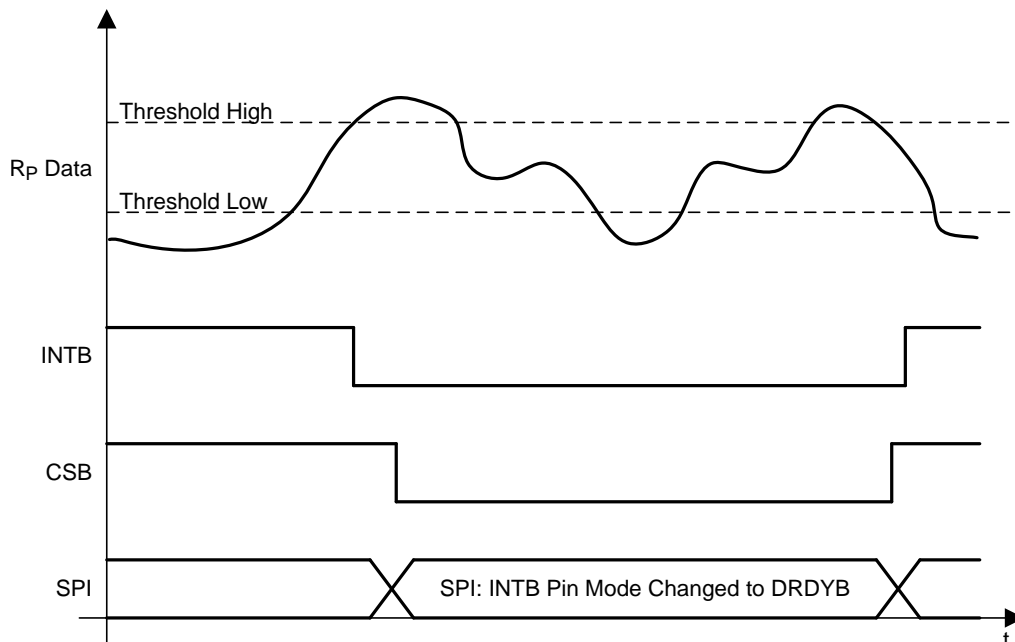


Figure 12. Behavior of INTB Pin in Wake-Up Mode

7.4.2.3 DRDY Mode

In DRDY mode, the INTB pin is asserted every time the conversion data is available and deasserted once the read command on register 0x21 is registered internally; if the read is in progress, the pin is pulsed instead. It is recommended to configure this setting after PWR_MODE has been set to 1 (the LDC1000 is in Active Mode).

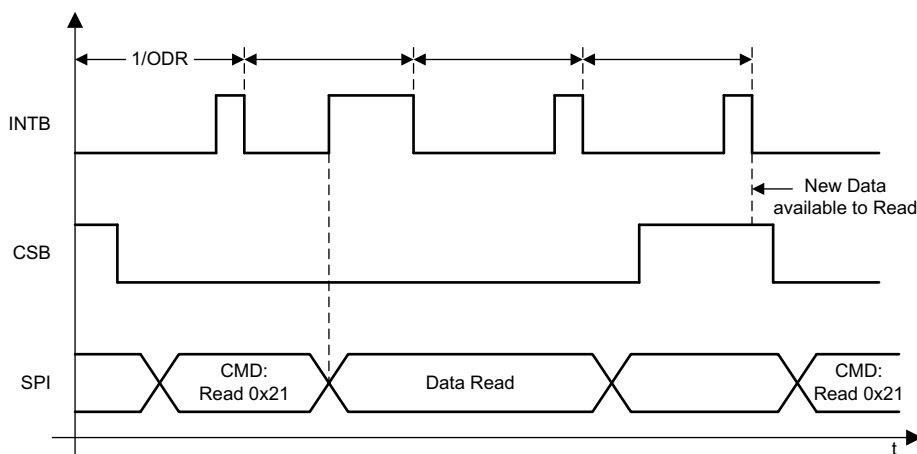


Figure 13. Behavior of INTB pin in DRDY Mode With SPI Extending Beyond Subsequent Conversions

Device Functional Modes (continued)

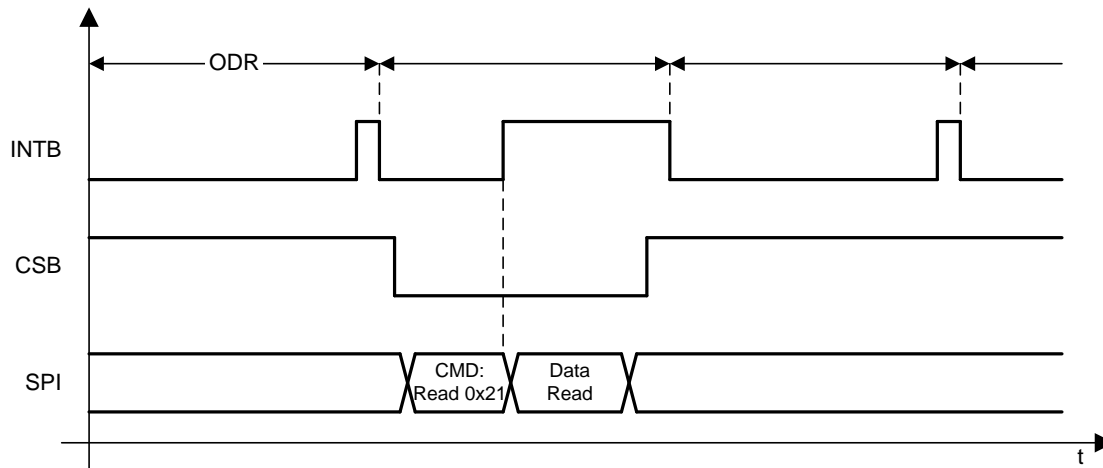


Figure 14. Behavior of INTB Pin in DRDY Mode With SPI Reading the Data Within Subsequent Conversion

7.5 Programming

The LDC1000 uses a 4-wire SPI to access control and data registers. The LDC1000 is a SPI slave device and does not initiate any transactions.

7.5.1 SPI Description

A typical serial interface transaction begins with an 8-bit instruction, which is comprised of a read/write bit (MSB, R=1) and a 7-bit address of the register, followed by a Data field which is typically 8 bits. However, the data field can be extended to a multiple of 8 bits by providing sufficient SPI clocks. Refer to the [Extended SPI Transactions](#) section below.

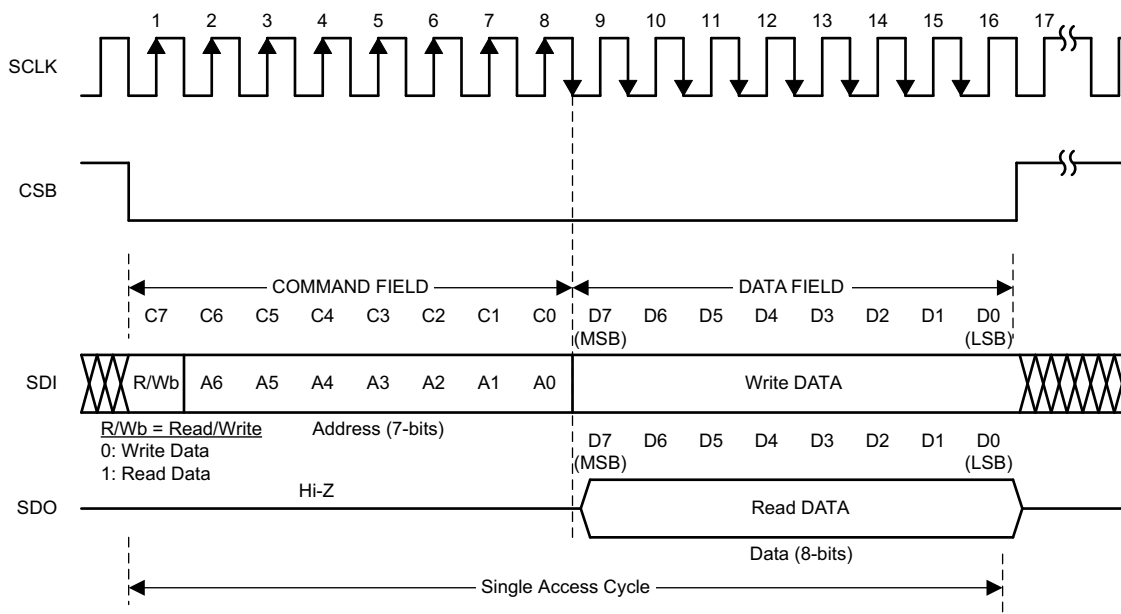


Figure 15. Serial Interface Protocol

Programming (continued)

Each assertion of chip select bar (CSB) starts a new register access. The R/Wb bit in the command field configures the direction of the access; a value of 0 indicates a write operation and a value of 1 indicates a read operation. All output data is driven on the falling edge of the serial clock (SCLK), and all input data is sampled on the rising edge of the serial clock (SCLK). Data is written into the register on the rising edge of the 16th clock. It is required to deassert CSB after the 16th clock; if CSB is deasserted before the 16th clock, no data write will occur.

The LDC1000 utilizes a 4-wire SPI interface to access control and data registers. The LDC1000 is an SPI slave device and does not initiate any transactions.

7.5.1.1 Extended SPI Transactions

A SPI transaction may be extended to multiple registers by keeping the CSB asserted for more than 16 pulses on SCLK. In this mode, the register addresses increment automatically. CSB must remain asserted during $8 \cdot (1+N)$ clock cycles of SCLK, where N is the amount of bytes to write or read during the transaction.

During an extended read access, SDO outputs the register contents every 8 clock cycles after the initial 8 clocks of the command field. During an extended write access, the data is written to the registers every 8 clock cycles after the initial 8 clocks of the command field.

Extended transactions can be used to read 16 bits of Proximity data and 24 bits of frequency data all in one SPI transaction by initiating a read from register 0x21.

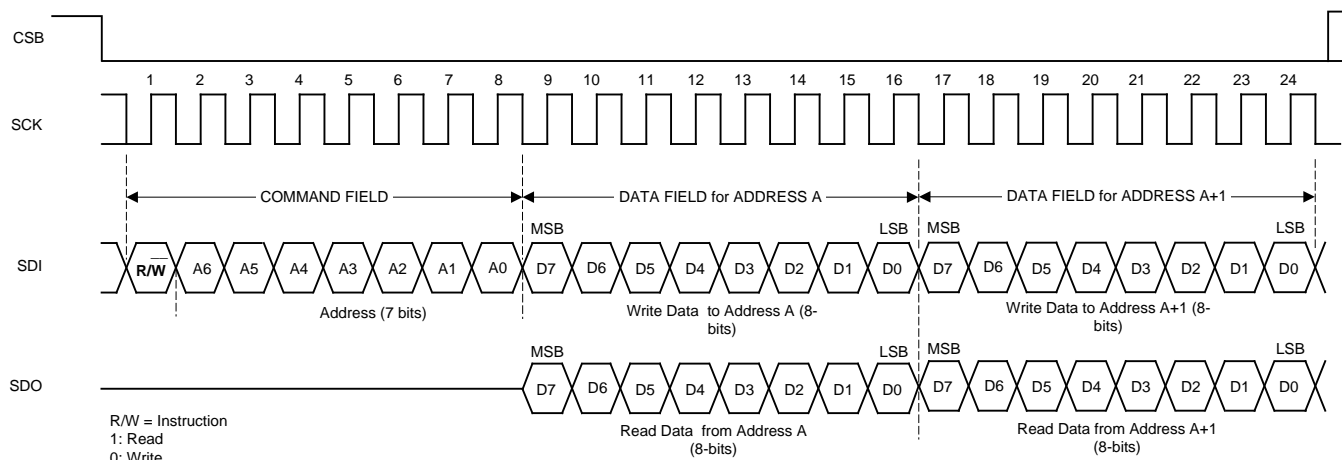


Figure 16. Extended SPI Transaction

7.6 Register Maps

Table 1. Register Description⁽¹⁾⁽²⁾⁽³⁾

| Register Name | Address | Direction | Default | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------------------------|---------|-----------|---------|--------------------------------|-------|---------|----------------|------------|---------------|-------------|--------------|
| Device ID | 0x00 | RO | 0x84 | Device ID | | | | | | | |
| R _P _MAX | 0x01 | R/W | 0x0E | R _P Maximum | | | | | | | |
| R _P _MIN | 0x02 | R/W | 0x14 | R _P Minimum | | | | | | | |
| Watchdog Timer Frequency | 0x03 | R/W | 0x45 | Min Sensor Frequency | | | | | | | |
| LDC Configuration | 0x04 | R/W | 0x1B | Reserved (000) | | | Amplitude | | RESPONSE_TIME | | |
| Clock Configuration | 0x05 | R/W | 0x01 | Reserved (00'0000) | | | | | | CLK_SE L | CLK_PD |
| Comparator Threshold High LSB | 0x06 | R/W | 0xFF | Threshold High LSB | | | | | | | |
| Comparator Threshold High MSB | 0x07 | R/W | 0xFF | Threshold High MSB | | | | | | | |
| Comparator Threshold Low LSB | 0x08 | R/W | 0x00 | Threshold Low LSB | | | | | | | |
| Comparator Threshold Low MSB | 0x09 | R/W | 0x00 | Threshold Low MSB | | | | | | | |
| INTB pin Configuration | 0x0A | R/W | 0x00 | Reserved (0'0000) | | | | | INTB_MODE | | |
| Power Configuration | 0x0B | R/W | 0x00 | Reserved (000'0000) | | | | | | | PWR_M ODE |
| Status | 0x20 | RO | | OSC Dead | DRDY | Wake-up | Compara tor | Don't Care | | | |
| Proximity | 0x21 | RO | | Proximity Data[7:0] Data LSB | | | | | | | |
| Proximity | 0x22 | RO | | Proximity Data [15:8] Data MSB | | | | | | | |
| Frequency Counter Data LSB | 0x23 | RO | | FCOUNT LSB | | | | | | | |
| Frequency Counter Data Mid-Byte | 0x24 | RO | | FCOUNT Mid Byte | | | | | | | |
| Frequency Counter Data MSB | 0x25 | RO | | FCOUNT MSB | | | | | | | |

(1) Values of register fields which are unused should be set to default values only.

(2) Registers 0x01 through 0x05 are Read Only when the part is awake (PWR_MODE bit is SET)

(3) R/W: Read/Write. RO: Read Only. WO: Write Only.

Table 2. Revision ID

| Address = 0x00, Default=0x80, Direction=RO | | |
|--|-------------|-------------------------|
| Bit Field | Field Name | Description |
| 7:0 | Revision ID | Revision ID of Silicon. |

Table 3. R_P_MAX

| Address = 0x01, Default=0x0E, Direction=R/W | | |
|---|------------------------|--|
| Bit Field | Field Name | Description |
| 7:0 | R _P Maximum | Maximum Sensor R _P that LDC1000 needs to measure. Configures the input dynamic range of LDC1000. See Table 4 for register settings. |

Table 4. Register Settings for R_P_MAX

| Register setting | R _P Maximum Sensor Drive (kΩ) |
|------------------|--|
| 0x00 | 3926.991 |
| 0x01 | 3141.593 |
| 0x02 | 2243.995 |
| 0x03 | 1745.329 |
| 0x04 | 1308.997 |
| 0x05 | 981.748 |
| 0x06 | 747.998 |
| 0x07 | 581.776 |
| 0x08 | 436.332 |
| 0x09 | 349.066 |
| 0x0A | 249.333 |
| 0x0B | 193.926 |
| 0x0C | 145.444 |
| 0x0D | 109.083 |
| 0x0E | 83.111 |
| 0x0F | 64.642 |
| 0x10 | 48.481 |
| 0x11 | 38.785 |
| 0x12 | 27.704 |
| 0x13 | 21.547 |
| 0x14 | 16.160 |
| 0x15 | 12.120 |
| 0x16 | 9.235 |
| 0x17 | 7.182 |
| 0x18 | 5.387 |
| 0x19 | 4.309 |
| 0x1A | 3.078 |
| 0x1B | 2.394 |
| 0x1C | 1.796 |
| 0x1D | 1.347 |
| 0x1E | 1.026 |
| 0x1F | 0.798 |

Table 5. R_P_MIN

| Address = 0x02, Default=0x14, Direction=R/W | | |
|---|------------------------|---|
| Bit Field | Field Name | Description |
| 7:0 | R _P Minimum | Minimum Sensor R _P that LDC1000 needs to measure. Configures the input dynamic range of LDC1000. See Table 6 for register settings. ⁽¹⁾ |

(1) This register needs a mandatory write as it defaults to 0x14.

Table 6. Register Settings for R_p_MIN

| Register setting | R _p Minimum Sensor Drive (kΩ) |
|------------------|--|
| 0x20 | 3926.991 |
| 0x21 | 3141.593 |
| 0x22 | 2243.995 |
| 0x23 | 1745.329 |
| 0x24 | 1308.997 |
| 0x25 | 981.748 |
| 0x26 | 747.998 |
| 0x27 | 581.776 |
| 0x28 | 436.332 |
| 0x29 | 349.066 |
| 0x2A | 249.333 |
| 0x2B | 193.926 |
| 0x2C | 145.444 |
| 0x2D | 109.083 |
| 0x2E | 83.111 |
| 0x2F | 64.642 |
| 0x30 | 48.481 |
| 0x31 | 38.785 |
| 0x32 | 27.704 |
| 0x33 | 21.547 |
| 0x34 | 16.160 |
| 0x35 | 12.120 |
| 0x36 | 9.235 |
| 0x37 | 7.182 |
| 0x38 | 5.387 |
| 0x39 | 4.309 |
| 0x3A | 3.078 |
| 0x3B | 2.394 |
| 0x3C | 1.796 |
| 0x3D | 1.347 |
| 0x3E | 1.026 |
| 0x3F | 0.798 |

Table 7. Watchdog Timer Frequency

| Address = 0x03, Default=0x45, Direction=R/W | | |
|---|----------------------|--|
| Bit Field | Field Name | Description |
| 7:0 | Min Sensor Frequency | <p>Sets the watchdog timer. The Watchdog timer should be set based on the lowest sensor frequency. If this field is set to too high a value, then the LDC1000 may incorrectly determine a sensor oscillation timeout.</p> $M = 68.94 \times \log_{10} \left(\frac{f_{\text{SENSOR}}}{2500} \right)$ <p>where:</p> <ul style="list-style-type: none"> f_{SENSOR} is the sensor frequency M is the register value to program for Min Sensor Frequency. <p>Example: With a Sensor frequency is 1 MHz Min Sensor Frequency=68.94*log₁₀(1×10⁶/2500)=Round to nearest integer(179.38) = 179</p> |

Table 8. LDC Configuration

| Address = 0x04, Default=0x1B, Direction=R/W | | |
|---|---------------|--|
| Bit Field | Field Name | Description |
| 7:5 | Reserved | Reserved to 000 |
| 4:3 | Amplitude | <p>Sets the oscillation amplitude</p> <p>00:1V 01:2V 10:4V 11:Reserved</p> |
| 2:0 | RESPONSE_TIME | <p>000: Reserved 001: Reserved 010: 192 011: 384 100: 768 101: 1536 110: 3072 111: 6144</p> |

Table 9. Clock Configuration

| Address = 0x05, Default=0x01, Direction=R/W | | |
|---|------------|--|
| Bit Field | Field Name | Description |
| 7:2 | Reserved | Reserved to 00'0000. |
| 1 | CLK_SEL | <p>Select Clock input type for L measurements.</p> <p>0: Clock input on XIN pin 1: Crystal connected across XIN/XOUT pins.</p> |
| 0 | CLK_PD | <p>Crystal Power Down.</p> <p>0: Crystal drive enabled. 1: Crystal drive is disabled. Use this setting to reduce power consumption with a crystal input when device is in Standby mode. Use this setting for clock input.</p> |

Table 10. Comparator Threshold High LSB

| Address = 0x06, Default=0xFF, Direction=R/W | | |
|---|----------------|---|
| Bit Field | Field Name | Description |
| 7:0 | Threshold High | Threshold High Register LSB. Combine with contents of register 0x07 to set upper threshold. |

Table 11. Comparator Threshold High MSB

| Address = 0x07, Default=0xFF, Direction=R/W | | |
|---|----------------|------------------------------|
| Bit Field | Field Name | Description |
| 7:0 | Threshold High | Threshold High Register MSB. |

Table 12. Comparator Threshold Low LSB

| Address = 0x08, Default=0x00, Direction=R/W | | |
|---|---------------|--|
| Bit Field | Field Name | Description |
| 7:0 | Threshold Low | Threshold Low Register LSB. Combine with contents of register 0x09 to set lower threshold. |

Table 13. Comparator Threshold Low MSB

| Address = 0x09, Default=0x00, Direction=R/W | | |
|---|---------------|-----------------------------|
| Bit Field | Field Name | Description |
| 7:0 | Threshold Low | Threshold Low Register MSB. |

Table 14. INTB pin Configuration

| Address = 0x0A, Default=0x00, Direction=R/W | | |
|---|------------|--|
| Bit Field | Field Name | Description |
| 7:3 | Reserved | Reserved to 00'000 |
| 2:0 | INTB_MODE | 000: All modes disabled. No signal output on INTB pin. 001: Wake-up Enabled on INTB pin 010: INTB pin indicates the status of Comparator output 100: DRDY Enabled on INTB pin All other combinations are Reserved |

Table 15. Power Configuration

| Address = 0x0B, Default=0x00, Direction=R/W | | |
|---|------------|---|
| Bit Field | Field Name | Description |
| 7:1 | Reserved | Reserved to 000'0000. |
| 0 | PWR_MODE | 0: Standby mode: LDC1000 is in a lower power mode but not actively converting. It is recommended to configure the LDC1000 while in this mode. 1: Active Mode. Conversion is Enabled Refer to Power Modes for more details. |

Table 16. Status

| Address = 0x20, Default=NA, Direction=RO | | |
|--|------------|---|
| Bit Field | Field Name | Description |
| 7 | OSC Status | 1:Indicates sensor oscillation timeout. This can be caused by a sensor with an R_p below R_{p_MIN} or setting Min Sensor Frequency too high. 0:Sensor oscillation timeout not detected. |
| 6 | Data Ready | 1:No new data available 0:Data is ready to be read |
| 5 | Wake-up | 1:Wake-up disabled 0:Wake-up triggered. Proximity data is more than Threshold High value. |
| 4 | Comparator | 1:Proximity data is less than Threshold Low value 0:Proximity data is more than Threshold High value |
| 3:0 | Don't Care | |

It is recommended to read register 0x21 immediately after any read of register 0x20.

Table 17. Proximity Data LSB

| Address = 0x21, Default=NA, Direction=RO | | |
|--|---------------------|--|
| Bit Field | Field Name | Description |
| 7:0 | Proximity Data[7:0] | Least Significant Byte of Proximity Data |

Conversion data is updated to the proximity register only when a read is initiated on 0x21 register. If the read is delayed between subsequent conversions, these registers are not updated until another read is initiated on 0x21.

Table 18. Proximity Data MSB

| Address = 0x22, Default=NA, Direction=RO | | |
|--|-----------------------|---|
| Bit Field | Field Name | Description |
| 7:0 | Proximity data [15:8] | Most Significant Byte of Proximity data |

Table 19. Frequency Counter LSB

| Address = 0x23, Default=NA, Direction=RO | | |
|--|--------------------------|--|
| Bit Field | Field Name | Description |
| 7:0 | FCOUNT LSB (FCOUNT[7:0]) | LSB of Frequency Counter. Sensor frequency can be calculated using the output data rate. Please refer to the Measuring Inductance With LDC1000 . |

Table 20. Frequency Counter Mid-Byte

| Address = 0x24, Default=NA, Direction=RO | | |
|--|--------------------------------|---------------------------------|
| Bit Field | Field Name | Description |
| 7:0 | FCOUNT Mid byte (FCOUNT[15:8]) | Middle Byte of Output data rate |

Table 21. Frequency Counter MSB

| Address = 0x25, Default=NA, Direction=RO | | |
|--|----------------------------|-------------------------|
| Bit Field | Field Name | Description |
| 7:0 | FCOUNT MSB (FCOUNT[23:16]) | MSB of Output data rate |

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Calculation of R_P_MIN and R_P_MAX

Different sensing applications may have a different range of the resonance impedance R_P to measure. The LDC1000 measurement range of R_P is controlled by setting 2 registers – R_P_MIN and R_P_MAX. For a given application, R_P must never be outside the range set by these register values, otherwise the measured value will be clipped. For optimal sensor resolution, the range of R_P_MIN to R_P_MAX should not be unnecessarily large. The following procedure is recommended to determine the R_P_MIN and R_P_MAX register values.

8.1.1.1 R_P_MAX

R_P_MAX sets the upper limit of the LDC1000 resonant impedance input range.

- Configure the sensor such that the eddy current losses are minimized. As an example, for a proximity sensing application, set the distance between the sensor and the target to the maximum sensing distance.
- Measure the sensor impedance R_P using an impedance analyzer.
- Multiply R_P by 2 and use the next higher value from [Table 7](#).

Note that setting R_P_MAX to a value not listed in [Table 7](#) can result in indeterminate behavior.

8.1.1.2 R_P_MIN

R_P_MIN sets the lower limit of the LDC1000 resonant impedance input range.

- Configure the sensor such that the eddy current losses are maximized. As an example, for a proximity sensing application, set the distance between the sensor and the metal target to the minimum sensing distance.
- Measure the sensor impedance R_P using an impedance analyzer.
- Divide the R_P value by 2 and then select the next lower R_P value from [Table 10](#).

Note that setting R_P_MIN to a value not listed on [Table 10](#) can result in indeterminate behavior. In addition, R_P_MIN powers on with a default value of 0x14 which must be changed to a value from [Table 10](#) prior to powering on the LDC.

8.1.2 Output Data Rate

The output data rate of (or the conversion time) LDC1000 depends on the sensor frequency, f_{sensor} and RESPONSE_TIME field in LDC Configuration register(Address:0x04). The maximum sample rate requires a RESPONSE_TIME setting of 192 and a sensor frequency of 5MHz.

$$SR = \frac{3 \times f_{\text{SENSOR}}}{\text{RESPONSE_TIME}} \quad (6)$$

8.1.3 Choosing Filter Capacitor (CFA and CFB Pins)

The filter capacitor is critical to the operation of the LDC1000. The capacitor should be low leakage, temperature stable, and it must not generate any piezoelectric noise (the dielectrics of many capacitors exhibit piezoelectric characteristics and any such noise is coupled directly through R_P into the converter). The optimal capacitance values range from 20 pF to 100 nF. The value of the capacitor is based on the time constant and resonating frequency of the sensor.

Application Information (continued)

If a ceramic capacitor is used, then a C0G (or NP0) grade dielectric is recommended; the voltage rating should be ≥ 10 V. The traces connecting CFA and CFB to the capacitor should be as short as possible to minimize any parasitics.

For optimal performance, the chosen filter capacitor, connected between pins CFA and CFB, needs to be as small as possible, but large enough such that the active filter does not saturate. The size of this capacitor depends on the time constant of the sense coil, which is given by L/R_S , (L =inductance, R_S =series resistance of the inductor at oscillation frequency). The larger this time constant, the larger filter capacitor is required. Hence, this time constant reaches its maximum when there is no target present in front of the sensor.

The following procedure can be used to find the optimal filter capacitance:

1. Start with a large filter capacitor. For a ferrite core coil, 10 nF is usually large enough. For an air coil or PCB coil, 100 pF is usually large enough.
2. Power on the LDC1000 and set the desired register values. Minimize the eddy currents losses, by minimizing the amount of conductive target covering the sensor. For an axial sensing application, the target should be at the farthest distance from coil. For a lateral or angular position sensing application, the target coverage of the coil should be minimized.
3. Observe the signal on the CFB pin using a scope. Because this node is very sensitive to capacitive loading, it is recommended to use an active probe. As an alternative, a passive probe with a 1 k Ω series resistance between the tip and the CFB pin can be used. The time scale of the scope should be set so that 10-100 cycles of the sensor oscillation frequency are visible. For example, if the sensor frequency is 1 MHz, the timescale per division of the oscilloscope should be set to 0.1ms.
4. Vary the values of the filter capacitor until that the signal observed on the CFB pin has an amplitude of approximate 1 V_{pp}. This signal scales linearly with the reciprocal of the filter capacitance. For example, if a 100 pF filter capacitor is applied and the signal observed on the CFB pin has a peak-to-peak value of 200 mV, the desired 1 V_{pp} value is obtained using a $200 \text{ mV} / 1 \text{ V} * 100 \text{ pF} = 20 \text{ pF}$ filter capacitor.

8.2 Typical Application

8.2.1 Axial Distance Sensing Using a PCB Sensor With LDC1000

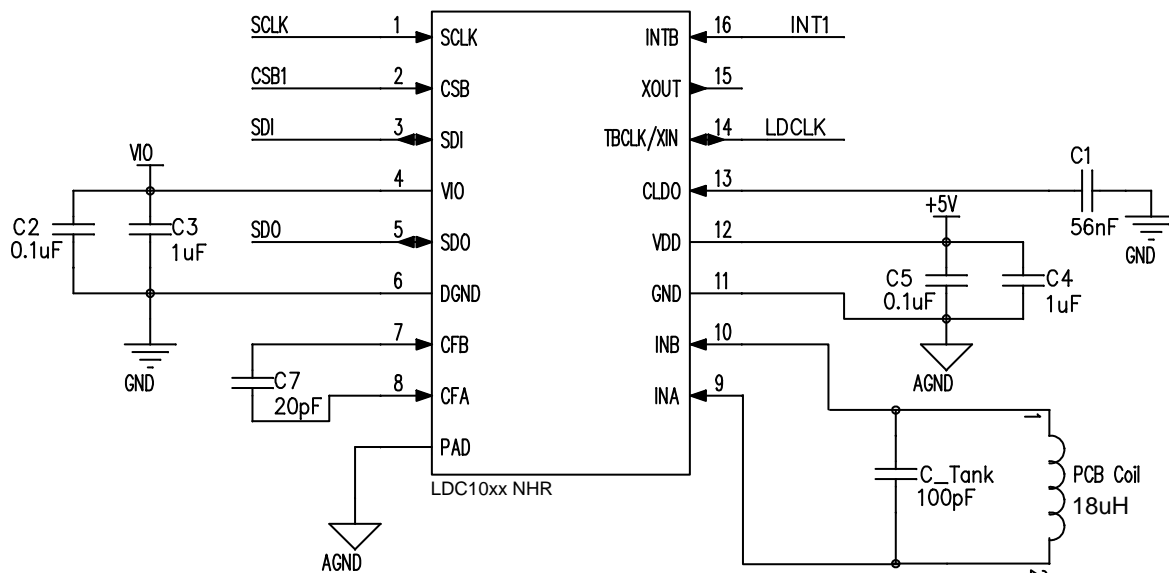


Figure 17. Typical Application Schematic, LDC1000

Typical Application (continued)

8.2.1.1 Design Requirements

For this design example, use the following as the input parameters.

Table 22. Design Parameters

| DESIGN PARAMETER | EXAMPLE VALUE |
|---------------------------------|--|
| Minimum sensing distance | 1 mm |
| Maximum sensing distance | 7 mm |
| Sample rate | 28 KSPS |
| Number of PCB layers for sensor | 2 layers with 62 mil (1.8mm) PCB thickness |
| Sensor Diameter | 551 mil (14 mm) |

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Sensor and Target

In this example, consider a PCB sensor with the below characteristics:

Table 23. Sensor Characteristics

| PARAMETER | VALUE |
|--|-----------------|
| Thickness of PCB copper | 1 Oz-Cu (35μm) |
| Coil shape | Circular |
| Number of turns | 23 |
| Trace thickness | 4 mil (0.102mm) |
| Trace spacing | 4 mil (0.102mm) |
| PCB core material | FR4 |
| R _p @ 1 mm target-sensor distance | 5 kΩ |
| R _p @ 7 mm target-sensor distance | 12.5 kΩ |
| Nominal sensor Inductance | 18 μH |

The target is a stainless steel disk of 15mm diameter and has a thickness of 1mm.

8.2.1.2.2 Calculating Sensor Capacitor

Sensor frequency depends on various factors in the application. For this example, one of the design parameters is a sample rate of 28 KSPS, which requires the sensor frequency as calculated below:

$$SR = \frac{3 \times f_{\text{SENSOR}}}{\text{RESPONSE_TIME}} \quad (7)$$

With an LDC1000 RESPONSE_TIME setting of 384 and output data rate specification of 28 KSPS, the sensor frequency would have to be 3.6 MHz.

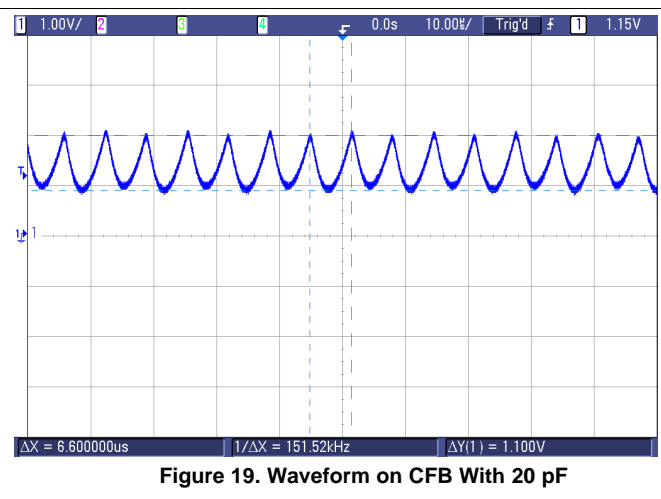
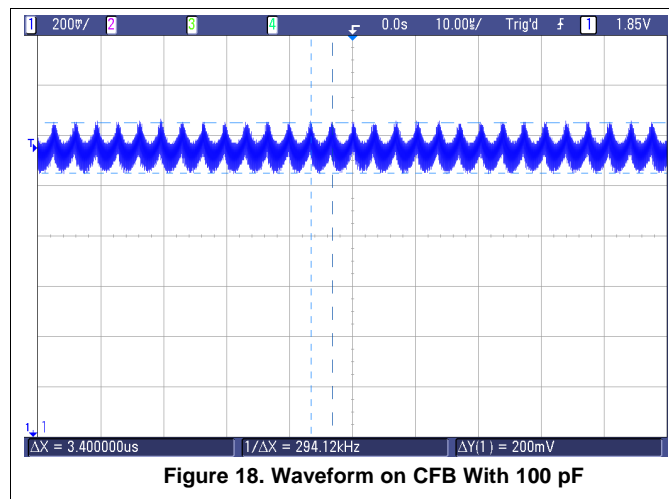
Now, using the below formula, the sensor capacitor is calculated to be 108 pF with the sensor inductance of 18 μH. A 100 pF sensor capacitor will slightly increase the sensor frequency to 3.75 MHz, and provide a sample rate of 29.3 KSPS.

$$L = \frac{1}{C \times (2\pi \times f_{\text{SENSOR}})^2} \quad (8)$$

As the target interacts with the sensor inductance, the apparent inductance will decrease. When the target is at the 1mm minimum distance for this application, the maximum interaction will occur, and the sensor frequency will increase to 3.95 MHz.

8.2.1.2.3 Choosing Filter Capacitor

Using the steps given in [Choosing Filter Capacitor \(CFA and CFB Pins\)](#), the filter capacitor for the example sensor is 20 pF. The waveform below shows the pattern on CFB pin with 100 pF and 20 pF filter capacitor. Notice that the timescale of scope traces is sufficient to view the waveform over many cycles of the sensor oscillation.



8.2.1.2.4 Setting R_{P_MIN} and R_{P_MAX}

Calculating value for R_{P_MAX} Register : R_P at 8 mm is 12.5 kΩ, 12500×2 = 25000. In [Table 7](#), then 27.704 kΩ is the nearest value larger than 25 kΩ; this corresponds to R_{P_MAX} setting of 0x12.

Calculating value for R_{P_MIN} Register : R_P at 1mm is 5 kΩ, 5000/2 = 2500. In [Table 6](#), 2.394 kΩ is the nearest value lower than 2.5 kΩ; this corresponds to R_{P_MIN} setting of 0x3B.

8.2.1.2.5 Calculating Minimum Sensor Frequency

Using

$$M = 68.94 \times \log_{10} \left(\frac{f_{\text{SENSOR}}}{2500} \right) \quad (9)$$

M is 218.96, which rounds to 219 decimal. This value should to be written into Watchdog Timer Register (address 0x03).

The LDC1000 includes a watchdog which monitors the sensor oscillation and flags an error in the STATUS register if no transitions occur on the sensor in a given time window. The time window is controlled by the Min Frequency setting. If the Min Sensor Frequency is programmed for too high a frequency, the watchdog will erroneously indicate that the sensor has stopped oscillating. If the Min Sensor Frequency is set too low, then the LDC1000 will take a longer time to detect if the sensor oscillation has stopped.

8.2.1.3 Application Curve

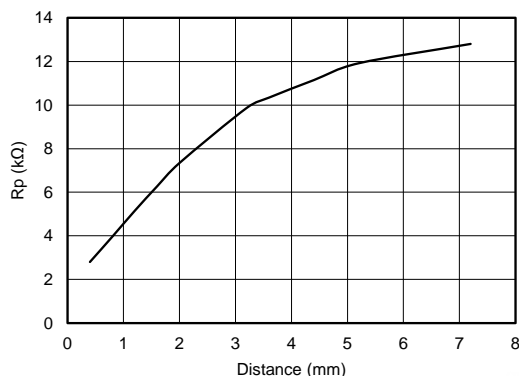


Figure 20. Rp vs Distance

9 Power Supply Recommendations

The LDC1000 is designed to operate from an analog supply range of 4.75 V to 5.25 V and digital I/O supply range of 1.8 V to 5.25 V. The analog supply voltage should be greater than or equal to the digital supply voltage for proper operation of the device. The supply voltage should be well regulated. If the supply is located more than a few centimeters from the LDC1000, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A capacitor with a value of 10 μ F is usually sufficient.

10 Layout

10.1 Layout Guidelines

- The VDD and VIO pin should be bypassed to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 0.1 μ F ceramic with a X5R or X7R dielectric. Some applications may require additional supply bypassing for optimal LDC1000 operation; for these applications the smallest-valued capacitor should be placed closest to the corresponding supply pin.
- The optimum placement is closest to the VDD/VIO and GND/DGND pins of the device. Take care to minimize the loop area formed by the bypass capacitor connection, the VDD/VIO pin, and the GND/DGND pin of the IC. See [Figure 21](#) for a PCB layout example.
- The CLDO pin should be bypassed to digital ground (DGND) with a 56 nF ceramic bypass capacitor.
- The filter capacitor selected for the application using the procedure described in section [Choosing Filter Capacitor \(CFA and CFB Pins\)](#) is connected between CFA and CFB pins. Place the filter capacitor close to the CFA and CFB pins. Do not use any ground or power plane below the capacitor and the trace connecting the capacitor and the CFA /CFB pins.
- Use of separate ground planes for GND and DGND is recommended with a star connection. See [Figure 21](#) for a PCB layout example.
- The sensor capacitor should be a C0G capacitor placed as close as possible to the sensor coil. Refer to [LDC Sensor Design App Note](#) for more details.

10.2 Layout Example

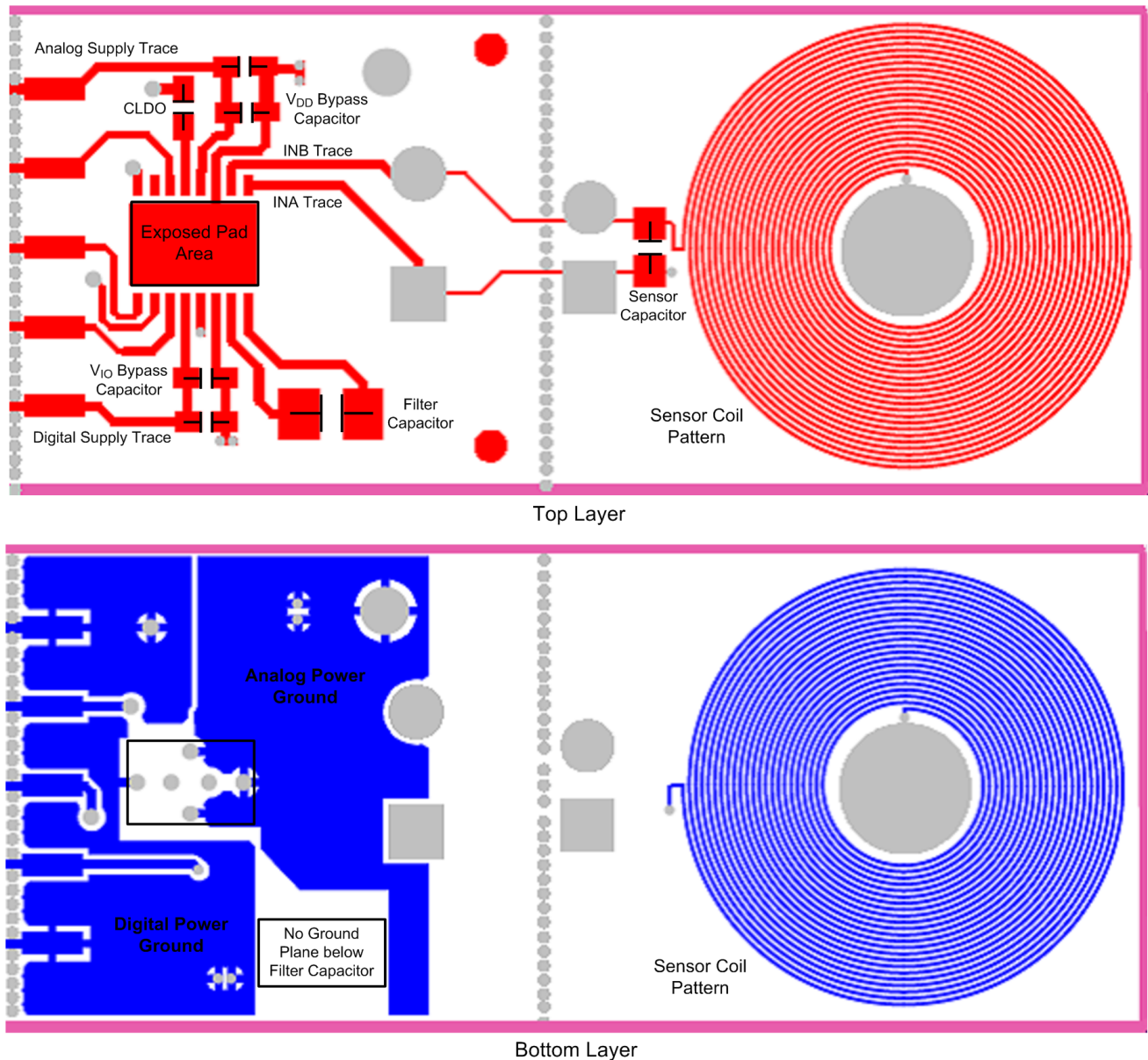


Figure 21. LDC1000 Board Layout

11 器件和文档支持

11.1 文档支持（如果适用）

11.1.1 相关文档

应用报告《IC 封装热指标》，[SPRA953](#)

《LDC 传感设计应用笔记》，[SNOA930](#)

11.2 社区资源

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11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

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| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| LDC1000NHRJ | ACTIVE | WSO | NHR | 16 | 4500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LDC1000 | Samples |
| LDC1000NHRR | ACTIVE | WSO | NHR | 16 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LDC1000 | Samples |
| LDC1000NHRT | ACTIVE | WSO | NHR | 16 | 250 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LDC1000 | Samples |

(1) The marketing status values are defined as follows:

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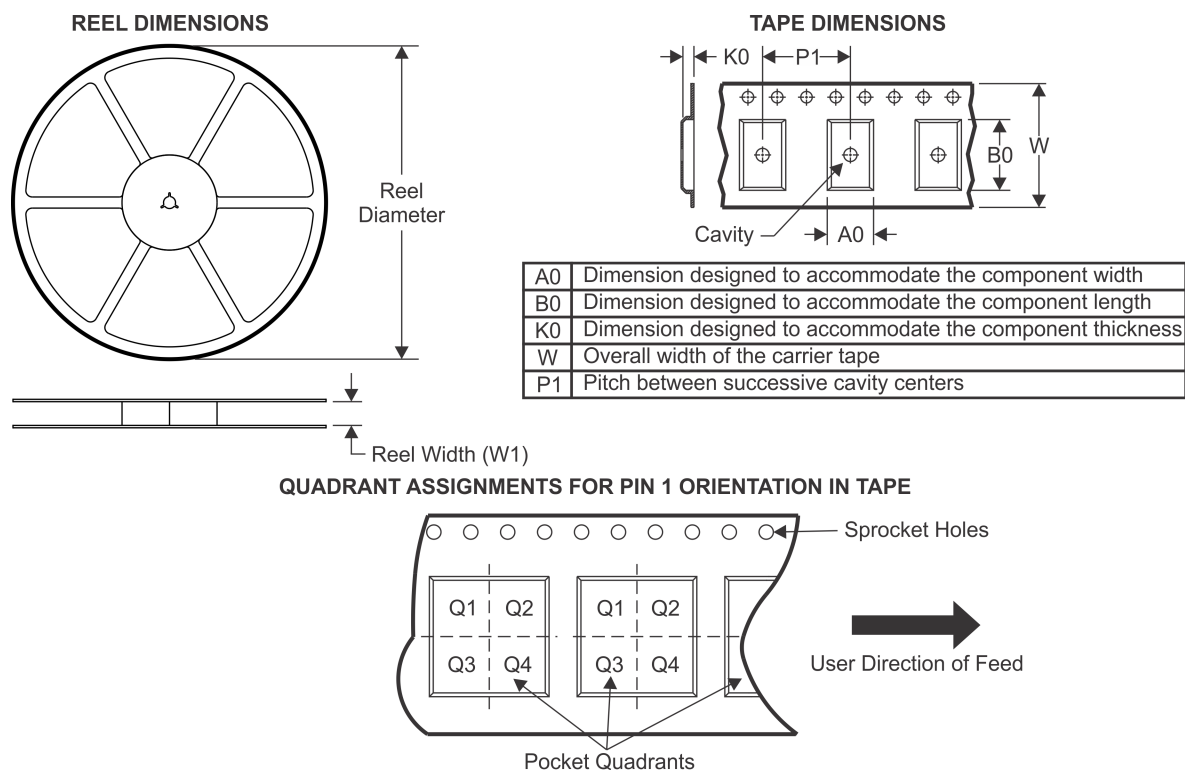
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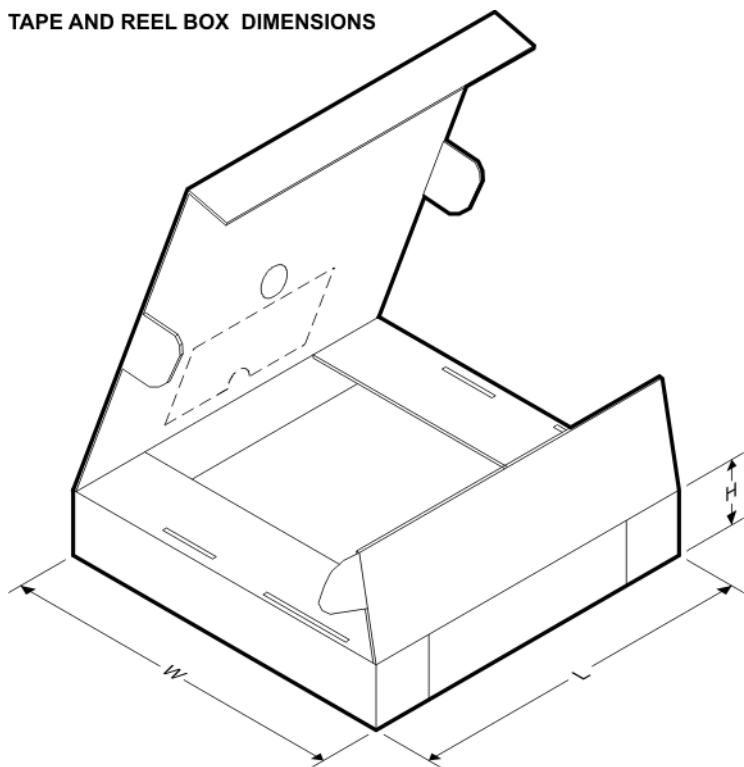
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

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*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LDC1000NHRJ | WSO | NHR | 16 | 4500 | 330.0 | 12.4 | 4.3 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LDC1000NHRR | WSO | NHR | 16 | 1000 | 178.0 | 12.4 | 4.3 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LDC1000NHRT | WSO | NHR | 16 | 250 | 178.0 | 12.4 | 4.3 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |

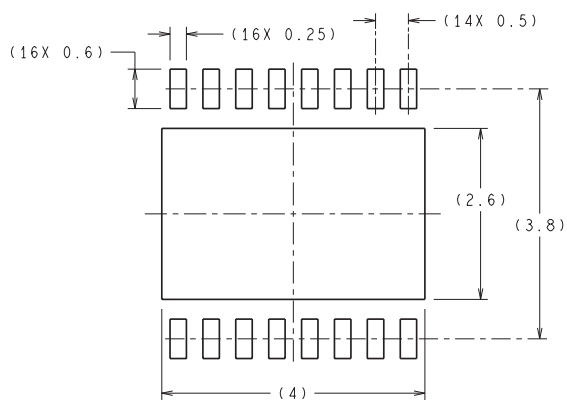
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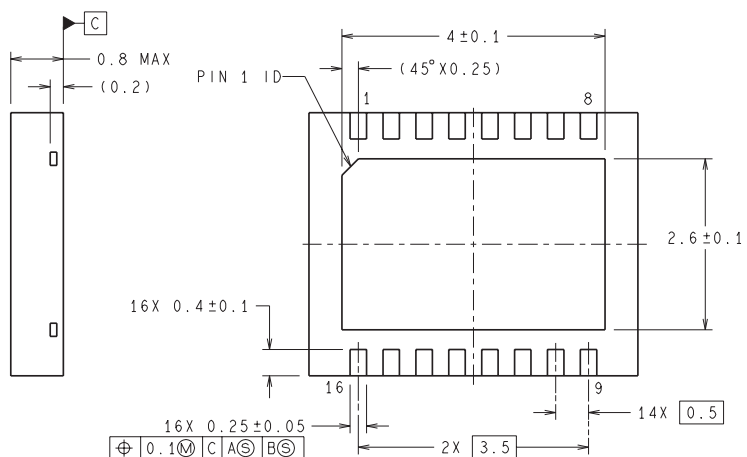
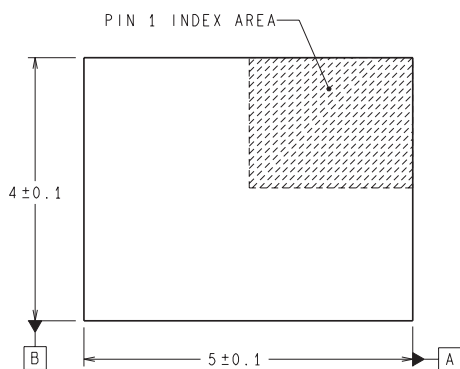
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|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LDC1000NHRJ | WSON | NHR | 16 | 4500 | 367.0 | 367.0 | 35.0 |
| LDC1000NHRR | WSON | NHR | 16 | 1000 | 210.0 | 185.0 | 35.0 |
| LDC1000NHRT | WSON | NHR | 16 | 250 | 210.0 | 185.0 | 35.0 |

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